Effect of Modulation Index on Switched Capacitor Based Inverter using PDD PWM

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Abstract— Power electronics semiconductor devices that are produces a sinusoidal voltage on many levels is called a multilevel inverter. They generate output that is more pristine and has lower harmonic distortion. The number of Switched Capacitor (SC) cells in this architecture determines the number of output levels, based on switched capacitor technology. By adjusting the capacitors in series and parallel, a lower voltage can be converted to a higher output. The circuit employs fewer components than a conventional switched capacitor multilevel inverter with the same architecture. Using Phase Delayed Disposition (PDD) PWM, inverter switching pulses are produced. Effect of frequency and amplitude modulation index are also examined in this paper in PWM techniques. At different modulation indices, the output voltage, Crest Factor, and %THD are assessed. The software used for the simulations is SIMULINK/MATLAB. The control mechanism is a crucial part of the circuit and is employed in conjunction with the PIC16F877A microcontroller to generate switching signals.

Keywords— Switched capacitor, single DC source, charging pump, and multilevel inverter

I. INTRODUCTION

Electric cars, distributed generation, electrical energy systems, and renewable energy sources like fuel cells and photovoltaic have all become increasingly important in the fight against environmental problems worldwide in recent years. In addition, it is expected that the power electronic equipment required for these systems—converters, inverters, etc.—would be able to manage bigger voltage and capacity ratings given the rate at which electrotechnic sectors are evolving. Multilevel inverters are one solution to this problem, because of their benefits in high power with low harmonic applications.

In contrast to a two-level inverter, a multilayer inverter produces an output phase voltage that is stepped and has a more complex harmonic profile [1]. Multilayer inverters perform power conversion in several voltage stages in order to provide higher voltage capability, improved electromagnetic compatibility, decreased switching losses, and superior power quality. Multilevel voltage source inverters come in three commercial topologies these days; the diode-clamped, flying capacitor, and cascaded H-bridge [1] designs are the most often used. Certain topologies, such as cascading H-bridges, employ several sources in order to achieve increased output levels. The challenge with diode clamped or neutral point clamped is that as the level rises, there are more clamping diodes. Similar to this, the flying capacitor multilayer inverter system gets larger as the number of capacitors grows. The cascaded H bridge inverter achieves the highest output voltage and power levels among these inverter topologies. The source voltage alone will be the output's highest amplitude value in each of the aforementioned topologies, with the remaining levels representing only a small portion of the input voltage.

A packed U-cell (PUC) inverter may output seven different voltage levels using 6 switches, single DC voltage source, and a capacitor whose voltage needs to be adjusted to fix at one-third of the first DC source [25]. The aforementioned topology requires less components than other topologies of seven level inverter [25]. The maximum output voltage level is the same as the input DC voltage alone.

Under typical circumstances, output voltage of the inverter is equals to its input voltage when the unity modulation index. A boost converter is used to raise the output levels, guaranteeing a larger load voltage [3]. As an alternative, we can employ inductors or transformers at the output side. A charge pump produces a voltage which is more than the input voltage by using switched capacitors [3]–[5]. The charge pump adds the one voltages over the input voltage sources and the capacitors [20]. A SC inverter produces multilayer voltage outputs by using switched capacitors. A charge pump and a SC inverter are similar in terms of topology. Figure 1 shows how a standard switched capacitor (SC) cell is converted into a suggested SCMLI. A standard SC cell includes three switching devices plus one capacitor; a modified SC cell has two switching devices, one diode, and one capacitor. Based on the Basic and Modified Inverter topologies, a new SC based Inverter is proposed. Proposed MLI is derived [3]–[10] to reduce the number of components and improve the THD spectrum.

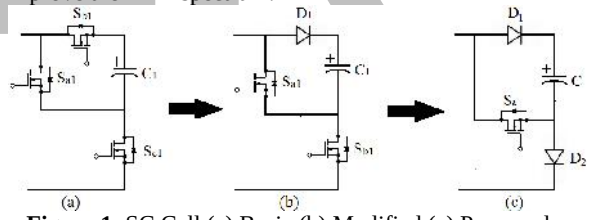

Figure 1: SC Cell (a) Basic (b) Modified (c) Proposed

Multicarrier Pulse Width Modulation is the primary method used to regulate multilevel inverter switches, and it can be used to lower the harmonic contents [6]. In order to generate switching pulses, Sinusoidal Pulse Width Modulation compares triangular carrier signals with sinusoidal modulating signals. The modulating signal's amplitude determines the PWM modulation index. The impact of varied modulation index on the maximum output voltage and the inverter's THD spectrum is examined.

II. SEVEN LEVEL INVERTER

A full bridge inverter and a SC network are the two structures that cascade to generate this high level switched-capacitor (SC) multilevel inverter [6]–[8]. The fundamental switching capacitor cell, as described in [10], is depicted in figure 2 and determines the level number at the load terminal. The primary benefit of this circuit is its extremely minimum switches in compared to other traditional topologies.

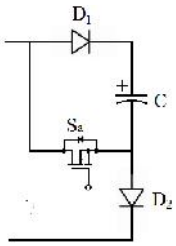

Figure 2: Basic Switched Capacitor Cell [10]

A cascade of N switched capacitor cells can create (2N+3) levels with a highest level of (N+1)V_{dc}. A basic SC cell having a capacitor, a switch, and 2 diodes, as shown in figure 2. Each block is designed for a parallel and series connection by properly switching the common switch S_b and the switch S_a. The forward biased diodes establish a parallel connection between the input and capacitor. An input source is in series with a SC capacitor when switch S_a is turned ON. These devices need to be switched correctly in order to receive the desired output.

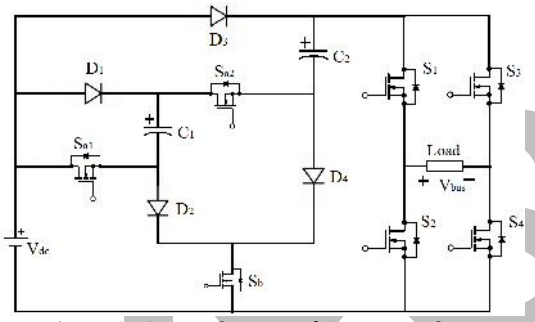

Figure 2: Circuit diagram of Seven Level Inverter

In this work, two switched capacitor cells are used to analyse a seven-level inverter. Every switched capacitor cell is connected to the voltage source through a switch S_b, as illustrated in Figure 3 and described in [10].With the elimination of the switched capacitor network, the aforementioned circuit operates as a standard H-bridge inverter, producing three output levels, the highest of which is the input DC voltage (V_{dc}). Two additional levels are produced in each half cycle and a maximum output level of $2V_{dc}$ is obtained by adding one switched capacitor module or cell with V_{dc} as the capacitor voltage.

Number of levels at output = 2N+3 (1)

Where N is the number of SC Module

III. WORKING MODES OF SEVEN LEVEL INVERTER

The multilevel inverter with switched capacitors that can generate up to seven levels is examined in this article; the circuit should use N=2 capacitor cells. When the capacitors are connected in parallel to the input voltage source, they start to accumulate charge. When the capacitors are connected in series with the input voltage source, they discharge [10]. The output of the switched capacitor network serves as the input for the single phase inverter.

A. Mode 1 (V_{bus} = 0 V)

All capacitors are generated in parallel with the input voltage source by turning on the switch Sb, which keeps an input voltage across each capacitor. Switches in the same upper/lower limb conduct to produce the zero voltage at the output shown in figure 4 when S2 and S4 or S1 and S3 are turned ON.

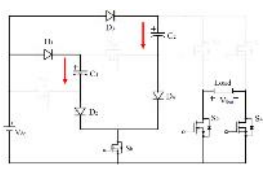

Figure 4: Mode 1

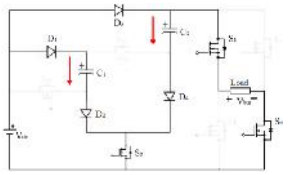

Figure 5: Mode 2

B. Mode 2 ($V_{bus} = V_{dc} - V_f$)

As shown in figure 5, where Vf is the forward voltage drop of diode D3, the first level, which is equal to (Vdc - Vf), is produced in this mode by turning on the full bridge inverter's switches S1 and S4. Additionally, turn on Switch SB so that the capacitor can be charged.

C. Mode 3 ($V_{bus} = V_{dc} + V_{C2} - V_f$)

When one capacitor is linked in series, this is the mode. Figure 6's switch Sa2 is simultaneously turned ON to connect the capacitor C2 in series with the source. During this time, the complete bridge inverter's switches S1 and S4 are conducting. Vdc + VC2 - Vf is the output voltage as a result. where VC2 is the voltage of capacitor C2 and Vf is the forward voltage drop of diode D1.

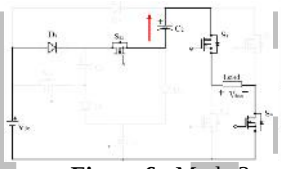

Figure 6: Mode 3

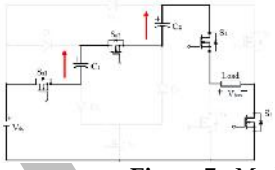

Figure 7: Mode 4

D. Mode 4 ($V_{bus} = V_{dc} + V_{C1} + V_{C2}$)

The two capacitors are connected in series in this manner. As seen in figure 7, the capacitors C_1 and C_2 are linked in series with the source voltage by connecting the switches S_{a1} and S_{a2}. During this time, the complete bridge inverter's switches S1 and S4 are operating. The voltage level that is left is (V_{dc} + V_{C1} + V_{C2}), where V_{C1} represents capacitor C_1's voltage and V_{C2} represents capacitor C_2's voltage.

As with S1 and S4, S2 and S3 can be set ON to produce the negative half cycle or OFF to provide the seven level output. Within the switched capacitor network, the input voltage determines the maximum voltage stress across each switch.

Table 1: Switching Sequences of Seven Level Inverter

LEVELS	S_1	S_2	S_3	S_4	S_{a1}	S_{a2}	S_b
0	0	1	0	1	0	0	1
V_{dc} - V_f	1	0	0	1	0	0	1
V_{dc} + V_{C2} - V_f	1	0	0	1	0	1	0
V_{dc} + V_{C1} + V_{C2}	1	0	0	1	1	1	0
- (V_{dc} - V_f)	0	1	1	0	0	0	1
- (V_{dc} − V_{C2} - V_f)	0	1	1	0	0	1	0
- (V_{dc} V_{C1} / V_{C2})	0	1	1	0	1	1	0

The switching pattern displayed in Table 1 can be used to demonstrate how the above topology operates in detail. The switches for each level in this table have values of 0 or 1, meaning that a switch with a value of 1 is in the ON state and a switch with a value of 0 is in the OFF state.

IV. PULSE WIDTH MODULATION SCHEMES

An effective modulation method is needed to regulate and generate an output waveform of good quality. The effectiveness of multicarrier PWM approaches is assessed using two parameters: frequency modulation ratio and amplitude modulation index [6]–[8].

The relation (2) defines the frequency ratio mf.

$$m_f = \frac{f_c}{f_m} \qquad (2)$$

Where, f_c is the carrier frequency of a triangle signal
f_m is the frequency of the modulating signal

The amplitude modulation index m_a is defined as

$$m_a = \frac{2A_m}{(m-1)\,A_c} \qquad (3)$$

Where, A_m is the modulating signal's amplitude,
A_c is the carrier signal's peak amplitude,
m is the number of output levels

A. Proposed Phase Delayed Disposition PWM (PDD PWM)

A novel PWM method called PDD PWM is employed to produce switching pulses for multilevel inverters. An n-level inverter continuously compares (n-1) carriers with the same carrier frequency (f_c) and peak-to-peak amplitude (A_c) to a sinusoidal reference waveform with amplitude A_m and reference frequency f_m. Figure 8 illustrates how the suggested sinusoidal Phase Delayed Disposition PWM (PDD) produces seven level output voltage using six triangular carrier signals. Carrier C_2 is 90^0 phases behind carrier C_1 in PDD, while carrier C_3 is 180^0 phases behind carrier C_1 in PDD. In a similar vein, carriers C_5 and C_6 phase delay from carrier C_4 by 90^0 and 180^0, respectively. Six carriers that are phase delayed are distributed evenly across the sinusoidal modulating signal.

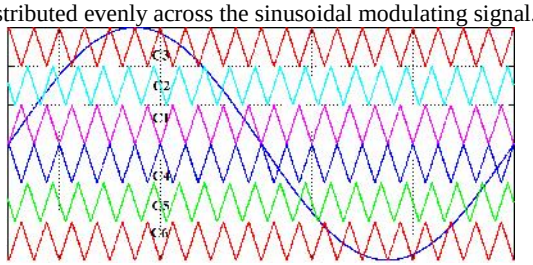

Figure 8: Phase Delayed Disposition PWM

All carriers are of same frequency and same amplitude but phase delayed and level shifted compared to other. PDD is a PWM which having the characteristic of conventional phase shifted and level shifted PWM.

B. Comparative Study with Other PWM Techniques

All of the carriers are in phase and disposed of in a continuous manner inside the bands they occupy in phase disposition (PD). Every carrier in the phase disposition method is in phase with every other carrier. In Phase Opposition Disposition (POD) modulation, all carrier waveforms above the sinusoidal zero reference are 180^0 out of phase with those below the zero reference. [6]. For each carrier waveform in alternate phase opposition disposition PWM (APOD), the phase shift is 180^0 relative to the carrier waveform next to it. The idea behind the Variable Frequency (VF) PWM approach is to use a single modulating waveform to carry many carriers at varying frequencies. Each carrier in this instance is in phase with the others, and they are arranged to occupy contiguous bands. Additionally, each carrier has a distinct frequency [6] [8] but the same amplitude. The overlapping vertical distance between each carrier in the carrier overlapping technique is half of the amplitude of one carrier amplitude. To accomplish this, arrange (n - 1) carriers so that the bands they occupy overlap one another.

Using various typical sinusoidal PWM approaches [6][8] for different switching frequencies, Figure 9 displays the %THD. THD for switching frequencies between 1 kHz and 50 kHz using sinusoidal PWM approaches ranges from 18% to 23%.

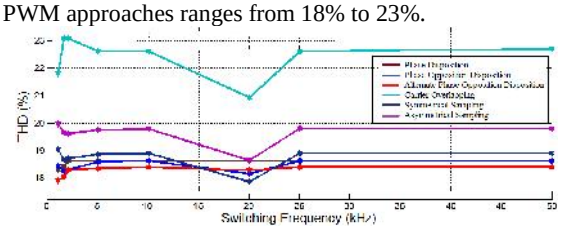

Figure 9: %THD Vs Switching Frequency for Sinusoidal Modulation

At 20kHz frequency %THD is reduced compared to other frequencies. This is due to the resonant condition formed by the switched capacitor with the load resistance.

The %THD utilising various Trapezoidal PWM methods is displayed in Figure 10. These PWMs are produced in accordance with the carrier signals listed above. Phase Disposition (PD) strategies demonstrate the lowest THD for all switching frequencies by utilising trapezoidal PWM algorithms. However, in contrast to sinusoidal PWM approaches, its THD levels are considerable.

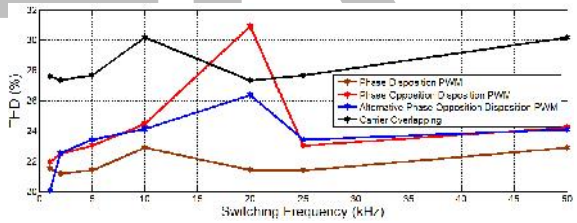

Figure 10: %THD Vs Switching Frequency for Trapezoidal Modulation

Figure 11 shows the %THD at various switching frequencies for PDD PWM technique. Compared to all other above mentioned PWM techniques PDD shows minimum %THD at 1kHz frequency. At 20kHz Switched Capacitor and load resistance forms a Resonant condition induces lower THD

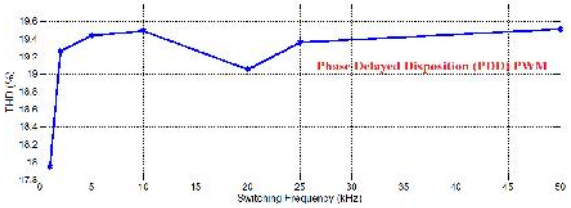

Figure 11: %THD Vs Switching Frequency

So by considering %THD proposed PDD PWM at 1kHz switching frequency is selected as the optimum control technique for the Switched Capacitor Inverter.

C. Switching Strategy for Switched Capacitor Cell

Every quarter cycle, a switched capacitor network experiences two switching scenarios. Figure 12 illustrates how each SC cell switch switches ON at a predefined angle (θi) in the first quarter cycle and OFF at a

corresponding angle (π-θi) in the second quarter cycle [20]. Every half cycle, these switching patterns are repeated. The SC cell's duty cycle is:

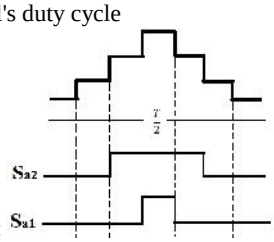

Figure 12: Switching Strategy for SC cell

$$D = \frac{T_{on}}{T/2} \quad (4)$$

Where, T_{on} = ON duration of Switch
T = Time period of Switching Pulse

The "FIRST ON LAST OFF" (FOLO) principle governs the switching pulses for the switched capacitor network (Sa1 & Sa2). This is because the first SC cell to turn ON will also be the last to turn OFF. And the last SC cell to turn ON will be the first to turn OFF [20].

V. SIMULATION ANALYSIS AND RESULTS

The SC seven level inverter was simulated using Matlab Ra2014a with an input of 5V, a switching frequency of 1kHz for fc, and a reference frequency of 50Hz for fm.

A. *Gate Pulse Generation*

Gate signals are obtained by comparing a sinusoidal reference or modulating signal at the fundamental frequency (50 Hz) with a triangular carrier signal, which is at a higher frequency. In this case, a switching frequency of 1 kHz or a carrier to fundamental frequency ratio of 20 is chosen for improved performance. Seven switching pulses utilizing the PDD PWM method are depicted in Figure 13.

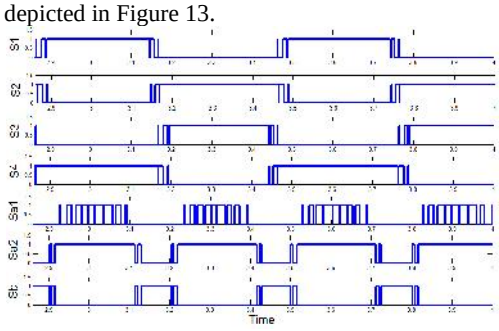

Figure 13: Switching Pulses using PDD techniques

B. *Capacitor Voltage*

It is important to choose a capacitor that can sustain the input voltage at the source. For low power applications, SC MLI is designed here. When S_{ai} is turned on, forward biased diodes allow capacitor C_i (i = 1,2....N) to begin charging to a voltage equal to (V_{dc}-2V_f). With a common switch S_b, two identical charging routes for each of the seven level inverter circuits ran in parallel to the DC input source. Each capacitor in a parallel connection has an equal charge. As seen in figure 14, the capacitor in this work is charged to 3.4V with V_{dc} = 5V and Forward diode drop of V_f = 0.8V.

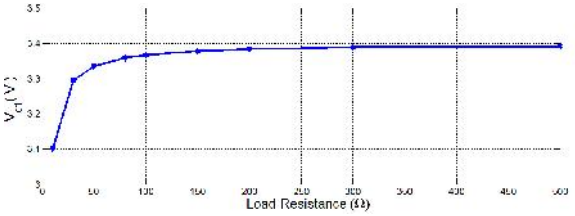

Figure 14: Capacitor Voltage

C. *Capacitor Voltage Ripple*

Fig. 15 displays the ripple in capacitor voltage variation with load resistance. Based on the plot, a ripple with a minimum value of 100Ω can be produced with a percentage less than 10%. When a load resistance greater than 100Ω is employed, the ripple in the capacitor will decrease correspondingly.

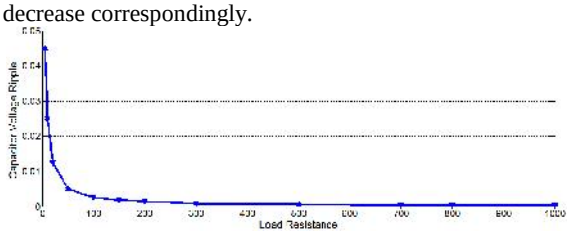

Figure 15: Capacitor Voltage Ripple Vs Load Resistance

D. *Load Voltage and current*

The load voltage of the seven-level topology is split into three stages. Since the load is linked across the input source and complete bridge switches are triggered, the input voltage must be determined first. The voltage at the subsequent stage is equal to the sum of the input voltage and the capacitor voltage. In a similar manner, the load voltage of the last level is equal to the total of the input and the voltages of all the series-connected capacitors. The seven-level voltage using the PDD PWM approach is shown in Figure 16. The maximum output voltage that may be achieved is 11.8V since the capacitor charges to 3.4V when fed a 5V DC input source.

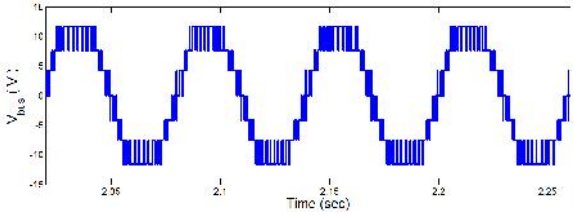

Figure 16: Output Voltage

Figure 17 shows the Seven level output current of the inverter with 100Ω resistance.

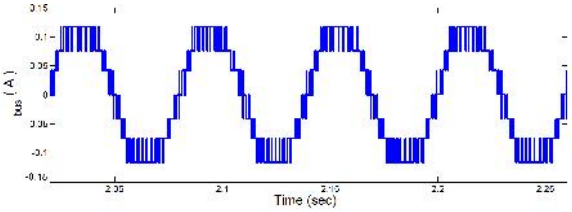

Figure 17: Output Current

E. *Variation of Output Voltage and THD with same input*

The output voltage and percentage THD for various level inverters with the same input voltage (V_{dc} = 5V) are displayed in Table 7.2. Output levels rise and %THD falls as the number of cells decreases. Table 2 makes it evident

that the suggested inverter produces increased output for a lower DC input.

Table 2: Variation of parameters for the same input

Input Voltage = 5V			
No of Cells	**No of Levels**	**Maxi Output Voltage**	**%THD at 1kHz**
0	3	4.2	51.74
1	5	8.36	28.49
2	7	11.7	17.9
3	9	14.87	13.71
4	11	17.8	11.74

F. Total Harmonic Distortion

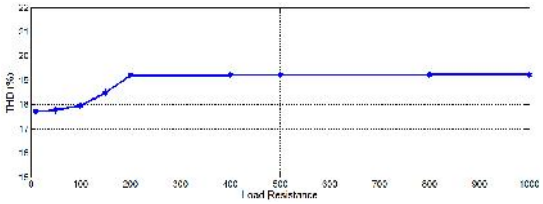

Figure 18: %THD Vs Load Resistance

The relationship between THD and load resistance is seen in Figure 18. The output's THD may change in response to changes in load resistance. The investigation shows that the THD became constant and independent of load resistance when resistance greater than 200Ω was applied.

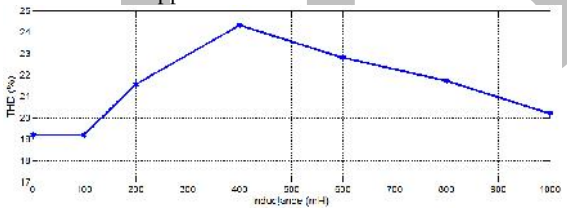

Figure 19: %THD Vs Load Inductance

The fluctuation of THD with inductance is depicted in Figure 19. For this variant, the load inductance is changed while the load resistance is fixed at 100 Ω.

G. Amplitude Modulation Index

The Modulation Index is adjusted between 0 and 1 based on the modulating signal A_m's amplitude measurement. The control method used in this study is set up to adjust the modulation index of the circuit depicted in figure 3 in order to generate three, five, and seven level inverter outputs.

Seven level output when $m_a \geq 0.7$

Five level output when $0.4 < m_a \leq 0.7$

Three level output when $m_a \leq 0.3$

Thus, the value of the Modulation Index influences THD. The fluctuation of %THD with modulation index is displayed in Figure 20. THD significantly drops as the number of levels rises with an increase in modulation index up to 1.

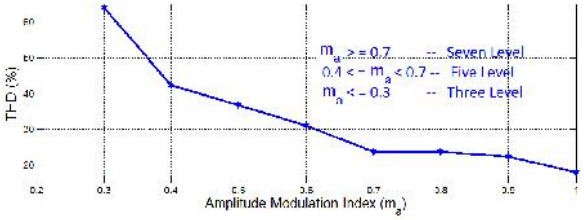

Figure 20: %THD Vs Modulation Index

Three level inverter is a full bridge with V_{dc} as the maximum level by taking modulation index m_a = 0.3 shown in figure 21.

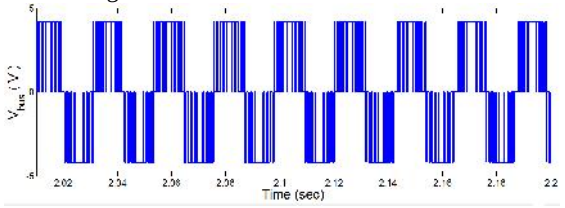

Figure 21: Three Level Output Voltage (m_a = 0.3)

In contrast, as seen in figure 22, a five-level inverter was created by joining a single switched capacitor cell to the entire bridge network, with (V_{dc}+V_{c1}) serving as the maximum voltage level and a modulation index of m_a = 0.6.

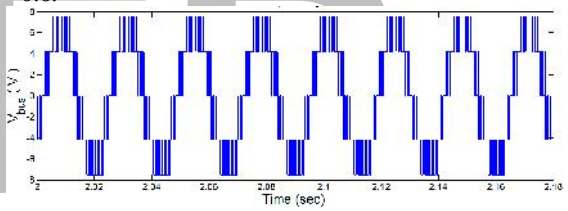

Figure 22: Five Level Output Voltage (m_a = 0.6)

Figure 23 illustrates the seven levels achieved by cascading two switched capacitor cells in parallel to the full bridge inverter, with the maximum voltage level being (V_{dc}+V_{c1}+V_{c2}) and a modulation index of m_a = 1.

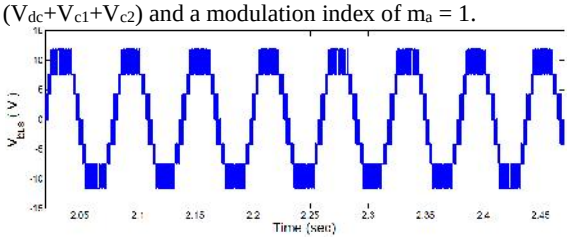

Figure 23: Seven Level Output Voltage (m_a = 1)

As more SC cells are added, the modulation index rises in conjunction, increasing the maximum output voltage and resulting in a variation in the number of levels. The fluctuation of the maximum output voltage with the modulation index is depicted in Figure 24. At the unity modulation index, the maximum output voltage and the lowest harmonic distortion are attained.

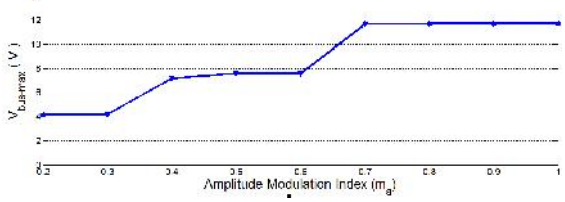

Figure 24: Maximum Output Voltage Vs Modulation Index

H. Frequency Modulation Index

The fluctuation of %THD with frequency modulation index mf is displayed in Table 3. At a frequency of 1 kHz or a frequency modulation index of 20, the minimum THD occurs. The ideal frequency for the seven level PDD inverter that is being proposed is 1 kHz.

Table 3: Variation of %THD with Frequency Modulation Index

Frequency Modulation Index m_f	Switching Frequency f_s (kHz)	%Total Harmonic Distortion (THD)
20	1	17.95
40	2	19.26
100	5	19.44
200	10	19.49
400	20	19.05
500	25	19.36
1000	50	19.51

I. Power Factor

It is equal to the cosine of the output voltage to current phase difference. Additionally, active power is the portion of total power (apparent power) that is used to perform useful labour. Current lags voltage for RL loads. Power factor is 0.9656 for the minimal load inductance of 1 mH and 0.9362 for the simulated value of 100 mH, as indicated in figure 25, with the same load resistance of 100 Ω.

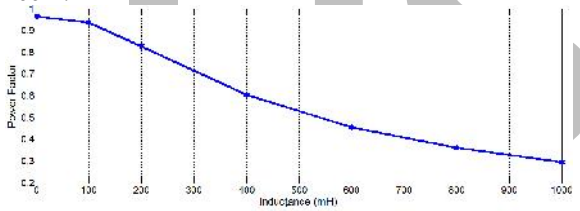

Figure 25: Power Factor Vs Load Inductance

J. Power Loss Vs Modulation Index

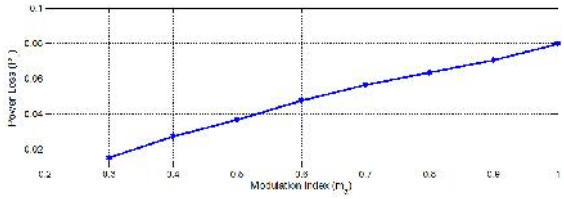

Figure 26: Power Loss Vs Modulation Index

The circuit illustrated in Figure 2 is made up solely of semiconductor switches, and the power loss that results from these switching losses is on the order of mill watts (mW). The circuit is configured as a 3-level inverter for 0.3 modulation index, with four H-bridge switches conducting and 15.41 mW of switching losses across these four switches. The modulation index circuit functions as a 5-level inverter with six switches active between 0.4 and 0.6. Similarly, when all 7 switches are in operation, a 0.7 to 1 modulation index 7-level output is created. Figure 26 illustrates how power loss increases as the modulation index rises. Because output voltage increases with increasing modulation index, output power also increases.

K. FFT Spectrum

With a modulation index of ma = 1, Figure 27 displays the output voltage's FFT spectrum utilizing the Phase Delayed Disposition PWM approach. In this case, 30 cycles of output voltage with a 50Hz fundamental frequency are taken into account for calculating %THD.

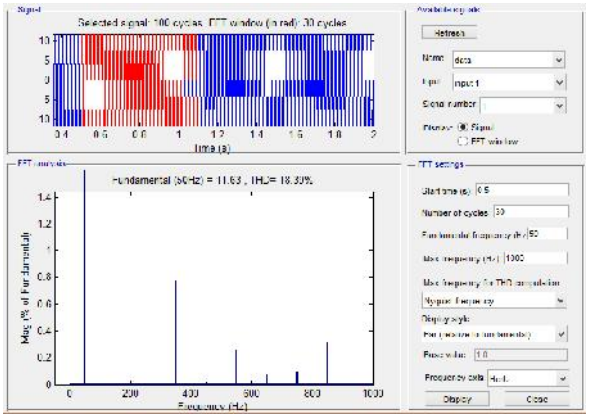

Figure 27: FFT Spectrum Output Voltage

L. Crest Factor

The instantaneous peak amplitude of a waveform divided by its root mean square value is known as the crest factor. The crest factor of the SC inverter for various modulation indices is displayed in Table 4.

Table 4: Crest Factor Vs Modulation Index

Level	Modulation Index	Crest Factor
7 Level	1	1.399
	0.9	1.546
	0.8	1.7414
	0.7	1.99
5 Level	0.6	1.5476
	0.5	1.667
	0.4	1.9845
3 Level	0.3	1.3258

The crest factor of a sinusoidal current waveform, equivalent to the current drawn by a pure resistive load, is 1.414. A genuine sinusoidal peak is 1.414 times the RMS value. According to Table 1, when Ma = 1, the crest factor is closer to the necessary value.

VI. COMPARATIVE STUDY

This chapter includes the comparative study of some multilevel inverter on the basis of number of components required [25]-[30].

The number of components needed to produce a single phase, seven-level output voltage waveform is shown in Table 5. Packed U Cell (PUC), one of these inverter topologies, requires less components to produce a 7-level output from a 5-level Packed U-Cell inverter [25][26][27]. However, no increased output is produced, and the capacitor must be charged to the necessary amount using a complicated capacitor balancing procedure.

Table 5: Components count for Single Phase 7-level Inverter

Inverter Type	DC Source V_{DC}	Capacitor	Diode	Active Switch	Control Circuit	Capacitor Balancing	Output Voltage Level	Step-Up Voltage
CHB [1][2]	3	3	0	12	Low	Easy	$8V_{dc}$	Yes
NPC [1][2]	1	6	10	12	High	Complex	$V_{dc}/2$	No
FC [1][2]	1	7	0	12	High	Complex	$V_{dc}/2$	No
PUC7 [25][26] Hybrid Seven Level [28]	1	3	4	8	High	Difficult	V_{dc}	No
E-Type [29] Step Up Inverter [30]	Seven Level not possible Seven Level not possible							
Basic SC 7 Level [3][8]	1	2	0	10	Low	Easy	$8V_{dc}$	Yes
Modified SC 7 Level [4]	1	2	2	8	Low	Easy	$8V_{dc}$	Yes
Proposed SC 7 Level [20]	1	2	4	7	Low	Easy	$8V_{dc}$	Yes

Compared to previous inverter topologies, the proposed switched capacitor inverter may provide boosted output from a small DC input and employs fewer switching components than other boosted inverters.

Table 6: Components count for Single Phase n-level Inverter

Inverter Type	DC Source	Capacitor	Diode	Active Switch
CHB	$\frac{n-1}{2}$	$\frac{n-1}{2}$	0	$2(n-1)$
NPC	1	$n-1$	$2(n-2)$	$2(n-1)$
FC	1	n	0	$2(n-1)$
PUC	1	$\sqrt{n-1}\ 1$	0	$2\sqrt{n-1}+2$
Hybrid MLI	1	$\frac{n-1}{2}$	$n-3$	$n+1$
E Type MLI	$\frac{n-1}{3}$	0	$\frac{5(n-1)}{6}$	$\frac{5(n-1)}{6}$
Step Up Inverter	1	$\frac{n-1}{2}$	$\frac{n-1}{2}$	$\frac{n+7}{2}$
Basic SCMLI	1	$\frac{n-3}{2}$	0	$\frac{3n-1}{2}$
Modified SCMLI	1	$\frac{n-3}{2}$	$\frac{n-3}{2}$	$n+1$
Proposed SCMLI	1	$\frac{n-3}{2}$	$n-3$	$\frac{n+7}{2}$

Table 6 is describes the number of components count for generalized structure having n-number of levels in the output. The minimum value that can substitute for n in the above table is 3.

Table 7: Components count for N module Single Phase Inverter

Inverter Type	DC Source	Capacitor	Diode	Active Switch	Possible Output Levels
CHB	N	N	0	4N	2N+1
NPC (N=1,3,5...)	1	N+1	2N	2N+2	N+2
FC (N=1,3,5...)	1	N+2	0	2N+2	N+2
PUC (Cascading PUC5) [27]	N	N	0	6N	4N+1
PUC (Cascading U Cell) [25][26]	1	N	0	2N+4	$(N+1)^2+1$
Hybrid MLI	1	N+1	2N	N+6	2N+3
E Type MLI	4N	0	10N	10N	12N+1
Step Up Inverter	1	2N	2N	2N+4	4N+1
Basic SCMLI	1	N	0	2N+4	2N+3
Modified SC MLI	1	N	N	2N+4	2N+3
Proposed SCMLI	1	N	2N	N+5	2N+3

Table 7 shows number of DC sources, Capacitors, Diodes,

Number of levels and semiconductor switches are determined by the number of units (N). There are two ways to cascade a packed U-cell inverter: (i) Packed U-Cell cascade [27] (ii) a single U-Cell cascaded. The alternative approach is to construct different levels utilising DC linkages, therefore it would have levels like 5, 10, 17, 26 [25]. The first method generates 5, 9, 13 levels [27]. The minimum level produced by the E-Type inverter [29] from a single module unit is 13, and the minimum level produced by the step-up inverter [30] is 5. For traditional Neutral Clamped and Flying Capacitor inverters, the number of module units can be changed in steps of 1, 3, 5, etc.

VII. EXPERIMENTAL SETUP AND RESULTS

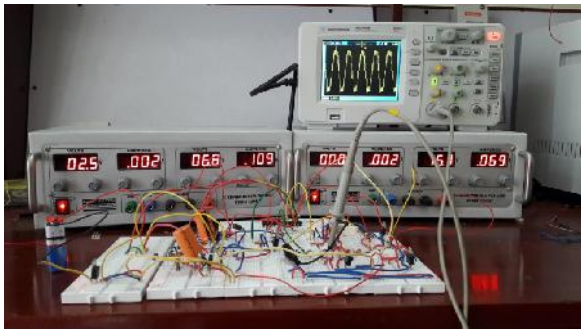

Figure 28: Experimental Setup of the Proposed Seven Level Inverter

The hardware setup for the seven-level inverter with switched capacitors is shown in Figure 28.

The PIC16F877A microcontroller uses the Phase Delayed Disposition PWM (PDD) approach to create pulses that control the MOSFET (IRF540). PDD provides a lower percentage of total harmonic distortion (THD) across all switching frequencies. With the help of an optocoupler TLP250 Driver/Optocoupler IC, these control pulses are amplified. The three-level voltage with ma= 0.3 is displayed in Figure 29.

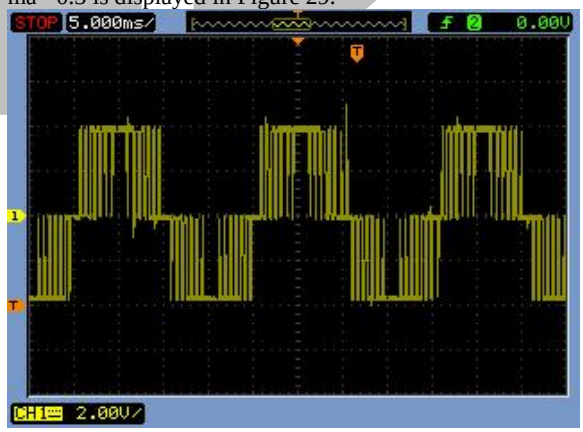

Figure 29: Experimental Result of Three Level Inverter

Figure 30 shows the five level voltage of the proposed topology with m_a= 0.6.

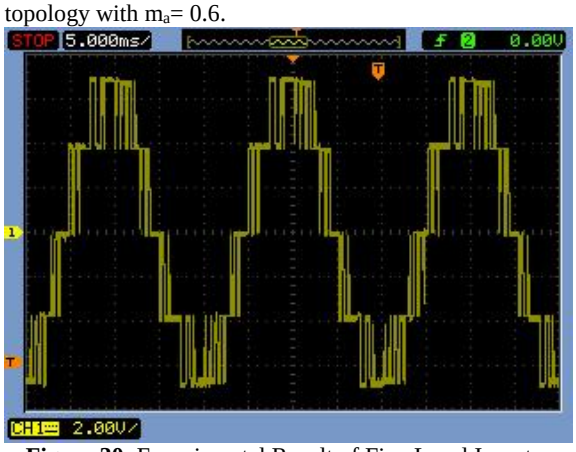

Figure 30: Experimental Result of Five Level Inverter

Figure 31 shows the seven level voltage of the proposed topology with m_a= 1.

Figure 31: Experimental Result of Seven Level Inverter

VIII.CONCLUSIONS

This study examines the impact of modulation index on a step-up SC seven-level inverter, which combines a complete bridge inverter with a DC–DC converter. There are many cascaded switched capacitor cells in a DC-DC converter. Comparing this multilayer inverter to switched capacitor multilevel inverters and regular inverters, you can see that it requires a very small number of switching components. A streamlined process for creating simulation models for multicarrier PWM methods using different modulating and carrier signals is demonstrated. Out of all the multicarrier PWM approaches, Phase Delayed Disposition (PDD) PWM delivers the least amount of THD. Operation and performance analysis of SC inverters is investigated based on seven-level prototype. It is possible to reach levels three, five, and seven by managing the modulation index varying from 0.3 to 1. An output level with the largest amplitude and the lowest percentage of overall harmonic distortion are produced by a control strategy with a unity modulation index. Additionally, under unity modulation index PWM control, the crest factor improves.

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